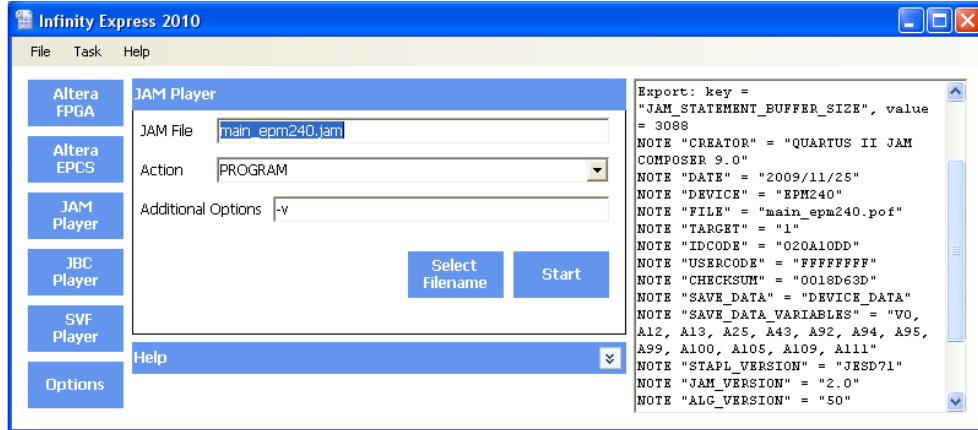




FEATURES

- Universal JTAG Programming using SVF or JAM files
- Altera FPGA configuration using CDF files generated by Quartus II
- In-System Programming of Altera EPCS configuration PROMs using RPD files generated by Quartus II
- Console commands allow full integration of software into user's GUI
- Works with **AP-114 ISP/JTAG Programming System**
- User programmable JTAG TCK speeds up to 10MHz
- Includes generic GDB Proxy Server
- Compatible with LabVIEW

INTRODUCTION

Infinity Express is the default application, and is provided free of charge with the **AP-114 ISP/JTAG Programming System**.

Together with the AP-114, **Infinity Express** offers a low cost, high-performance solution for all JTAG programming applications, replacing the various types of device specific In-System/JTAG programmers with a single Universal Hardware platform, expandable with the various software packages according to the required application.

This includes a replacement for the Altera ByteBlaster II system, allowing Altera FPGAs and EPCS Serial Configuration devices to be programmed using the appropriate CDF or RPD file.

Like all Infinity applications, the software is accessed via the **Infinity Launch Pad**, which enables users to keep track of their current software version, and check for any upgrades, as well as access recent files and support documentation.

Infinity Express offers Universal JTAG programming using industry standard SVF and JAM/STAPL files. All devices that are compatible with SVF or STAPL are supported by the SVF/JAM Players respectively.

Additionally, Jam-Byte Code (JBC) files can also be used to program PLDs, memories, and other compliant devices in a JTAG chain.

An indicative JTAG device support list can be found on our website at www.atomicprogramming.com/download

Each application within Infinity Express can be accessed via Console command lines, and therefore easily integrated into the users own system without the need to use the Infinity Express GUI.

As with all Atomic Programming software, Infinity Express is compatible with LabVIEW

JAM & JBC PLAYERS

STAPL (Standard Test and Programming Language) is a high level language designed specifically for CPLD ISP programming. It is the JEDEC standard version of the original Jam Language created by Altera.

The Jam player utility takes a JAM/STAPL File and applies vectors for programming and testing devices in a JTAG scan-chain. Embedded system developers can also use the JAM Player to program devices in their system. .

A STAPL "composer" is required to create the JAM/STAPL file, which is done as a stand-alone utility or as part of an integrated software tool (e.g. Altera Quartus, Xilinx iMPACT etc.)

The Jam-Byte Code (JBC) File is simply a different implementation of the Jam/STAPL file.

It is a binary version of the JAM/STAPL File which is in ASCII text format. Like Jam/STAPL files, all Data & Programming/Test algorithms are contained within the JBC file. The files are compiled using a JBC Compiler - which takes a standard format JAM file created by the Altera Quartus II software, for example, and converts them into the JBC file. This binary implementation results in smaller file sizes and shorter programming times.

The JBC Player is used to program JBC files into programmable logic devices (PLDs), memories, and other compliant devices in a JTAG chain.

The JBCPlayer is also able to read and "play" older Jam Byte-Code files based on Jam v1.1 syntax.

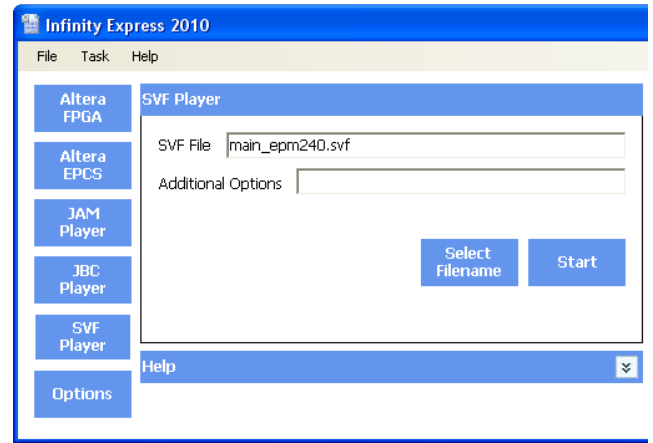
All devices that are compatible with Jam/STAPL are supported.

SVF PLAYER

The SVF Player takes Serial Vector Format (SVF) files and uses them to program or test most JTAG-compliant devices.

An SVF file would be created using a stand-alone utility or as part of an integrated software tool (e.g. Altera Quartus, Xilinx iMPACT etc.).

Generally, SVF format files are used when programming ISP devices via JTAG during in-circuit test flow using Automatic Test Equipment (ATE). Because of the way the file format is constructed, SVF files produce longer programming times for CPLDs. It's also sequential ASCII text file format - it does not support loops, resulting in very large sequential based files. As a whole SVF would really only be used for CPLDs if you were planning to production program CPLD devices through in-circuit testers.



ALTERA-SPECIFIC SUPPORT

ALTERA FPGA

This application is specific to Altera devices and duplicates the functions provided by the Altera ByteBlaster II system. It is targeted for embedded JTAG configuration. It enables configuration files to be tested before programming into Serial Configuration EPROM devices. The software driver allows configuration of Altera's FPGAs in JTAG mode, using Raw Binary File (.RBF) format input files. A Chain Description File (.CDF) generated by the Quartus II software is also required.

ALTERA EPCS

This application is specific to Altera EPCS Serial Configuration devices and is targeted at embedded Serial Configuration device programming. It is used for in-system (ISP) programming Altera Devices EPCS1, EPCS4, EPCS16, EPCS64 & EPCS128.

The software takes Raw Programming Data (RPD) format files, which are generated by the Altera Quartus II software, and programs the data into the selected serial configuration device.

GDB Proxy Server

Also built into Infinity Express is a GDB proxy server that translates commands from GDB such as read memory, read registers and set breakpoints and converts them into JTAG sequences that can be used to access actual hardware.

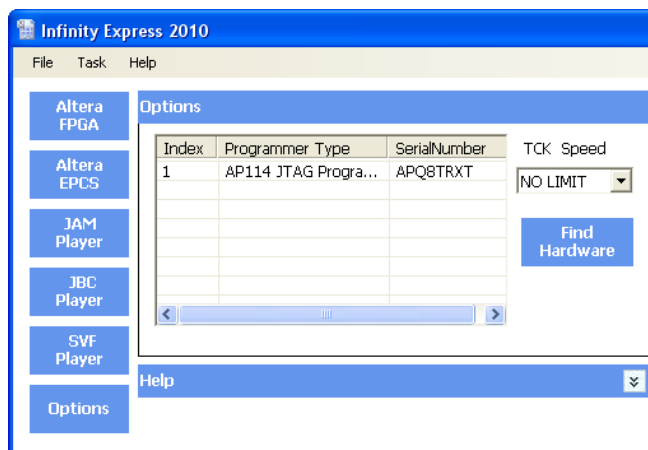
GDB (GNU project debugger) is an open standard and any debugger supporting GDB may be connected to the GDB proxy server using socket communication.

It allows you to see what is going on 'inside' another program while it executes, or what another program was doing at the moment it crashed

OTHER FEATURES

OPTIONS

Use the Options tab to set the JTAG TCK Clock Speed for the required application. This can be done separately using the **-s** option in the individual programs.

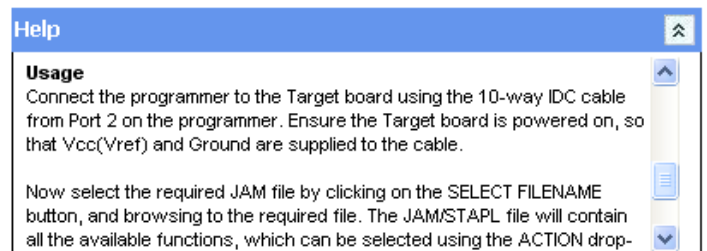


The **Find Hardware** button scans the USB port(s) to search for all connected programmers. Each programmer will be listed, with its assigned ID code and unit serial number. Up to 16 programmers can be connected in a daisy-chain.

This serial number can be used as an option within each application to target specific programmers for specific requirements. Clicking on required programmer shown on the list sets the **-p** option within each of the applications

HELP

Help text is available for each of the applications. Simply click on toggle arrows and the Help screen opens to explain how each application works.



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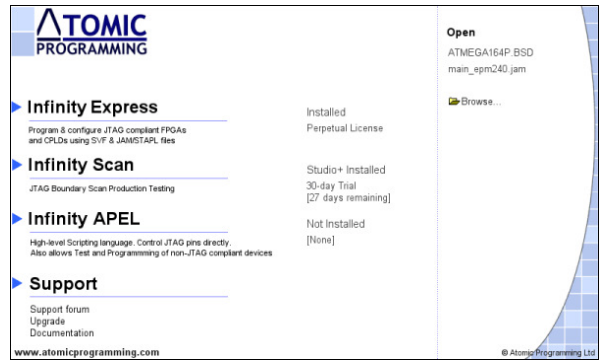
INFINITY SUITE

Infinity Express is part of a suite of JTAG tools that provides complete board test coverage.

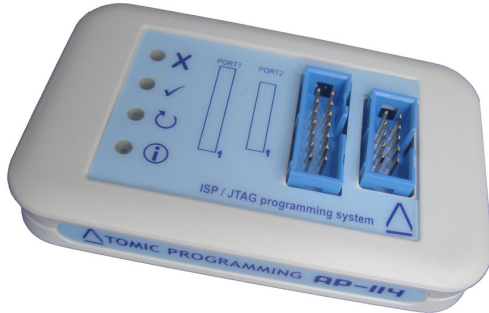
Infinity Scan provides a powerful JTAG Boundary Scan function, with plug-ins giving full support for Production applications.

Infinity APEL, with its own Embedded Script language, provides comprehensive functional testing and debugging of boards, including non-JTAG devices.

Each application is run from **Infinity Launch Pad**, which enables users to keep track of their current software version, check for any upgrades, as well as access recent files and support documentation.



UNIVERSAL HARDWARE PLATFORM



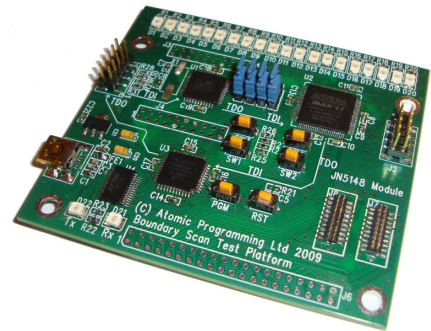
The **AP-114 ISP/JTAG Programming System** provides a single, portable, all-in-one solution for In-System Programming (ISP) of both JTAG and non-JTAG devices, Boundary Scan Testing, JTAG debugging and out of system device programming.

All applications within the **Infinity Suite** are supported by the **AP-114**, and with the range of supplied cable assemblies, supports any required JTAG pinout up to 14-pins. No other hardware is required for running the Infinity Suite. The **AP-114** supports JTAG, SPI, I2C and Microwire interfaces

The **AP-114** is supplied as standard with **Infinity Express**, and also comes with the **Infinity Program** software for universal In-System Programming (ISP) of EEPROM and SPI Flash memory, plus Atmel AVR and Microchip PIC microcontroller devices.

JTAG TRAINING PLATFORM

The JTAG Training Platform is an ideal solution for Educational use and general equipment training. It provides everything required to help your understanding of JTAG Boundary scan testing, FPGA configuration and JTAG debugging. Additionally, the platform also develops knowledge of ISP programming of Atmel AVR microcontrollers and SPI memory, and can be used as a development kit for Jennic JN5148 wireless microcontroller modules.



ATOMIC PROGRAMMING

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